**Module 1**

1. Summarize the importance of verification with respect to present day technology.
2. Describe functional verification. List and explain different types of functional verification.
3. Explain about the significance of human factor in design verification.
4. What is formal verification? Explain the various techniques used for performing the formal verification.
5. Write short notes on
6. Test benches
7. Re-convergence model
8. Discuss about
9. Scan based testing and design
10. Design and verification reuse
11. Compare VLSI testing versus verification.
12. Discuss about cost of verification and its influencing factors.
13. What do you mean by lint check in VLSI verification? Elaborate its advantages and disadvantages.
14. Explain linting of VHDL and Verilog source codes with suitable examples.
15. What is a simulator? Explain event driven and cycle based simulating tools with examples.
16. Discuss about co-simulators. Analyze the issues related to Co-simulation verification process.
17. Classify code coverage verification tool. Explain any three coverage types with suitable examples.
18. Discussabout

i).Waveform viewers

ii) Hardware modelers

1. Mentionthe types of code coverage tool.Explainstatement coverage and path coverage with examples.

Module2

1. Explain the verification process with respect to different design levels of the present day technology.
2. Describe the functionality of a test bench. Differentiate directed testing and random testing in verification.
3. What do you mean by hardware verification language? Compare HDL with HVL.
4. What do you mean by a layered test bench? Explain it in detail with a suitable example.

1. **i)** Write a note on simulation environment phases. ii) Elaborate on the built-in data typesavailable in System Verilog
2. Illustrate the basic array operations available in System Verilog with suitable examples.
3. Illustrate how to create new objects in system verilog with examples.
4. Explain string task and string operators with an example.
5. i) Elaborate on how to choose a storage type in system verilog

ii) Discuss about creating user defined data structure with examples

1. Elaborate on how to choose a best data structure in system verilog.
2. Explain the basic array operation for and for each with a suitable examples.
3. Write a descriptive note on i) dynamic arrays ii) queues
4. Mention the array methods supported in system verilog. Explain array reduction method in detail
5. Elaborate on array locator method with an example.
6. Explain the concept of array sorting and ordering in system verilog
7. Illustrate the concept of building a scoreboard with array locator methods.

Module3

1. Explain Procedural statements supported in System Verilog

2. Write a System Verilog code using break and continue while reading a file

3. Briefly discuss about Tasks, Functions and Void Functions in System Verilog.

4. Show how an argument can be passed by the reference. Explain how default argument values are used with an example

1. Summarize the advantages of using interface in connecting DUT and testbench.
2. Elaborate on controlling timing of synchronous signals with a clocking block.
3. With a suitable example explain driving interface signals through a clocking block.
4. Discuss about (i) Bidirectional signals in the interface (ii) Specifying delays in clocking blocks.
5. Discuss about the clock generator with suitable programs.
6. Elaborate on i) protocol exceptions, errors and violations. ii) feedback from functional coverage to stimulus.
7. Explain the concept of top-level scope considering the arbiter design.

Module4

1. Elaborate on the features of Object oriented programming (OOP) available in System Verilog
2. Illustrate with suitable examples the process of copying an object with a new operator.
3. Give the comparison of static and global variables.
4. Illustrate out-of block routine declaration with an example
5. Elaborate on the concept of class routines in System Verilog
6. Discuss how a routine can be defined outside the class with a suitable example
7. Elaborate on the scoping block and scoping rules
8. How do you refer a variable out of scope? Illustrate with System Verilog code.
9. Discuss about passing objects and handles to methods in System Verilog
10. Explain the concept of copying objects in System Verilog
11. Explain the transaction class with pack and unpack functions.
12. With the help of a neat diagram,explain the concept of building a layered test bench in System Verilog

Module5

1. What do you mean by randomization in System Verilog? Explain which parameters can be randomized.
2. Develop a random array of unique values in System Verilog.
3. Elaborate on randomization features in System Verilog
4. Write a explanatory note on constraint details in System Verilog.
5. What are the issues encountered when creating a random stimulus
6. How is randomization done in system Verilog? Explain with an example code
7. What are the different constraint styles available in system Verilog
8. Elaborate on constraint gaurds with suitable example code.
9. What do you mean by iterative constraints in System Verilog? Explain in detail
10. Write a note on solution probabilities available in System Verilog
11. How do achieve weighted distribution of variables System Verilog? Explain.